SiP vs. SoC
WiFi and Beyond

WIRELESS FUTURE. UNLEASHED NOW.™

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Agenda

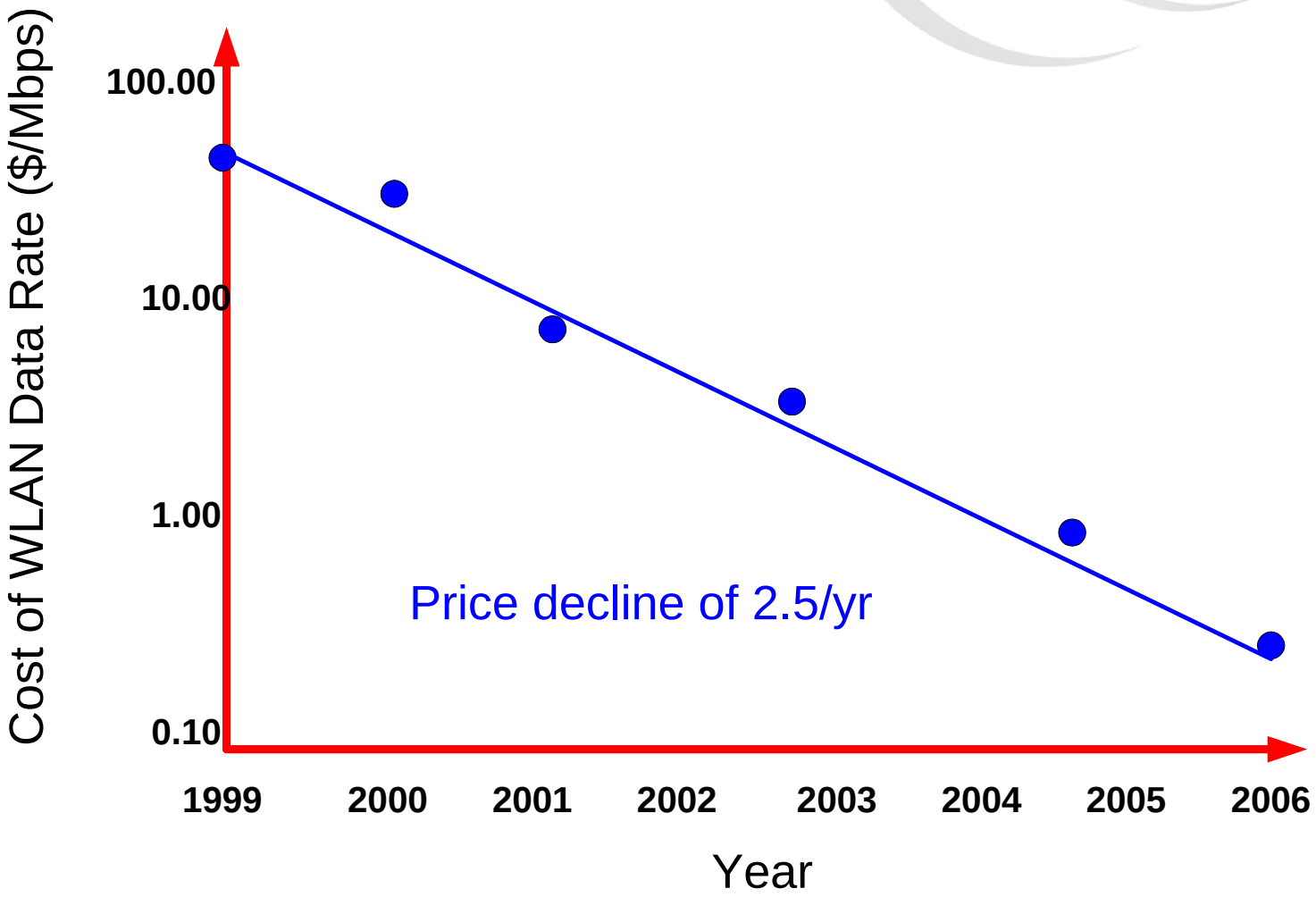
- System in a Package vs. System on a Chip: History and Trends
- Atheros, a RoC company
- SiP Market Drivers
- Are SiPs in Your Future?
- Summary

SiP vs. SoC: History and Trends

SoC: History & Trends

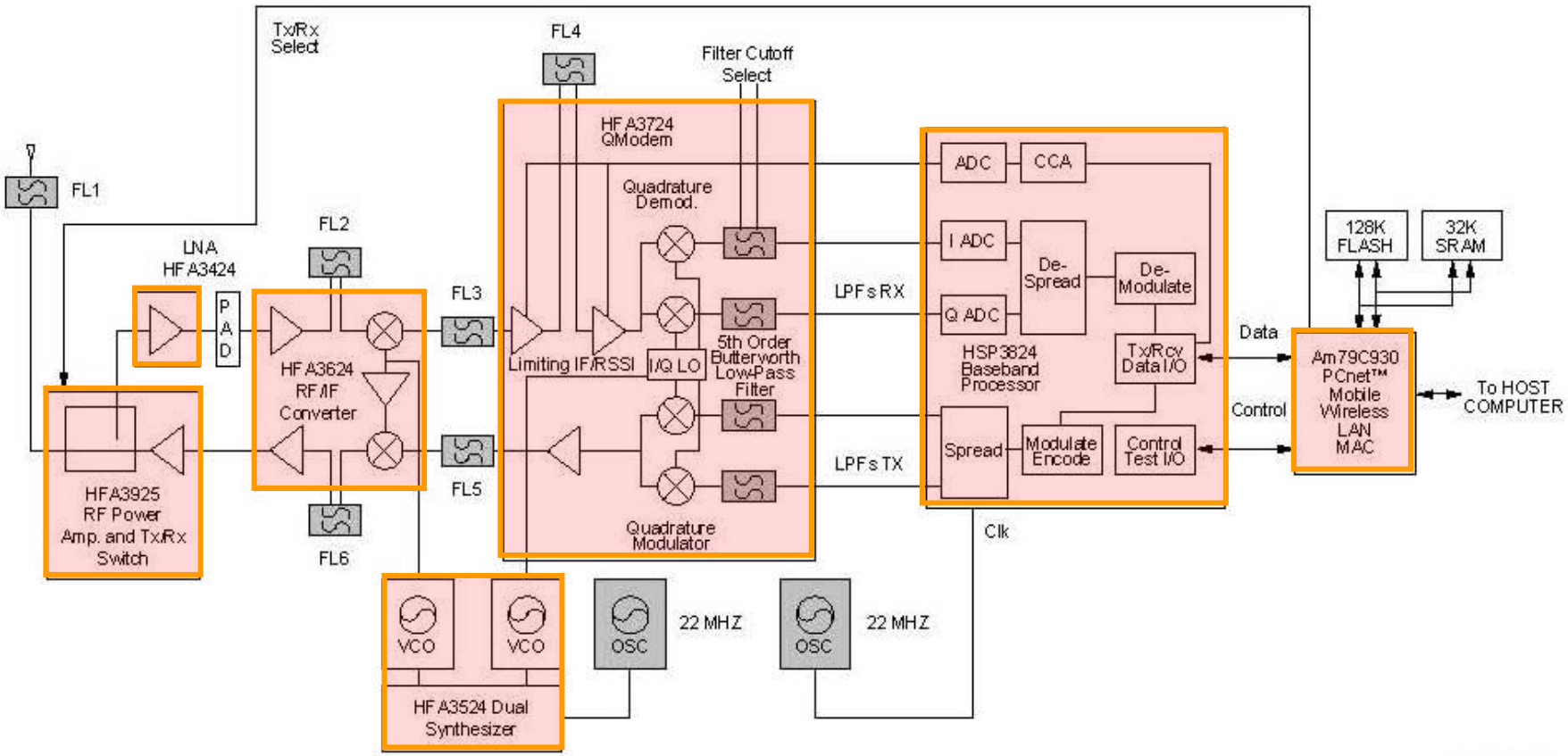
- 5 Main drivers of the semiconductor industry
  - Cost
  - TTM
  - Features/Performance
  - Power
  - Size
- Feature/Complexity/Performance ↑ ⇨ TTM/Power/Size ↑
- WiFi: 11b →11g →11a/b/g (dual concurrent) →11n
- Cost/Mbps vs. time ↓↓

Cost of WiFi Throughput



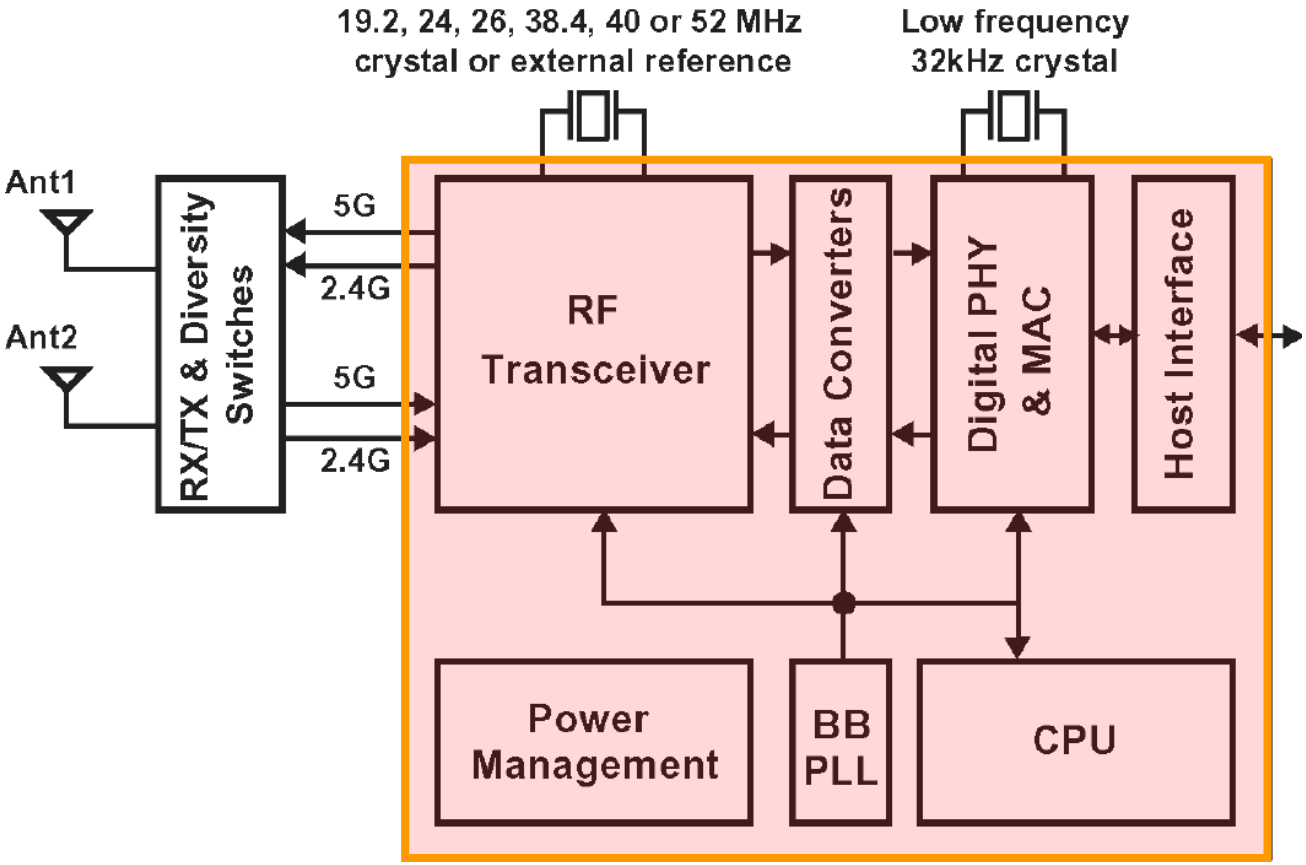
source: Zargari et al, RFIC 2005

Technology Progression: WiFi 1996



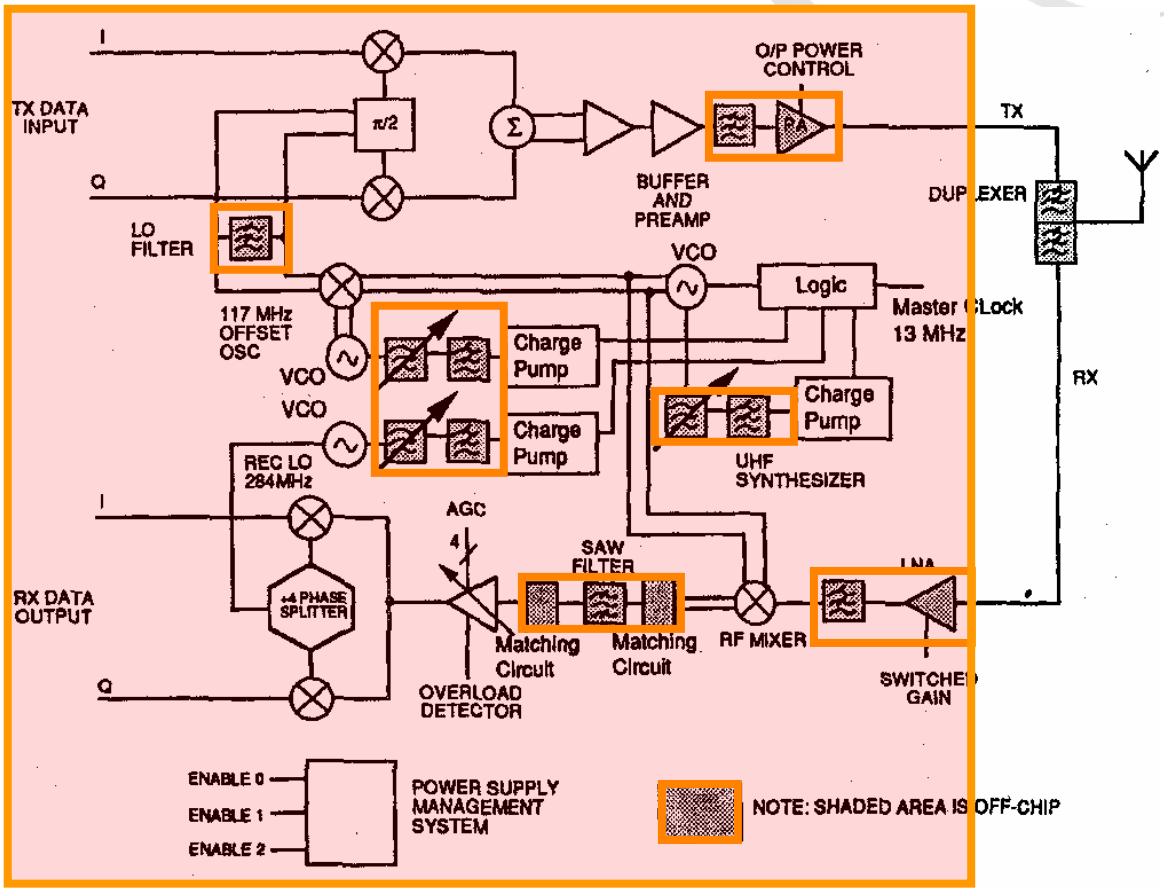
Harris 802.11b Chipset

WiFi: Today (2005)



Atheros 802.11a/b/g SoC

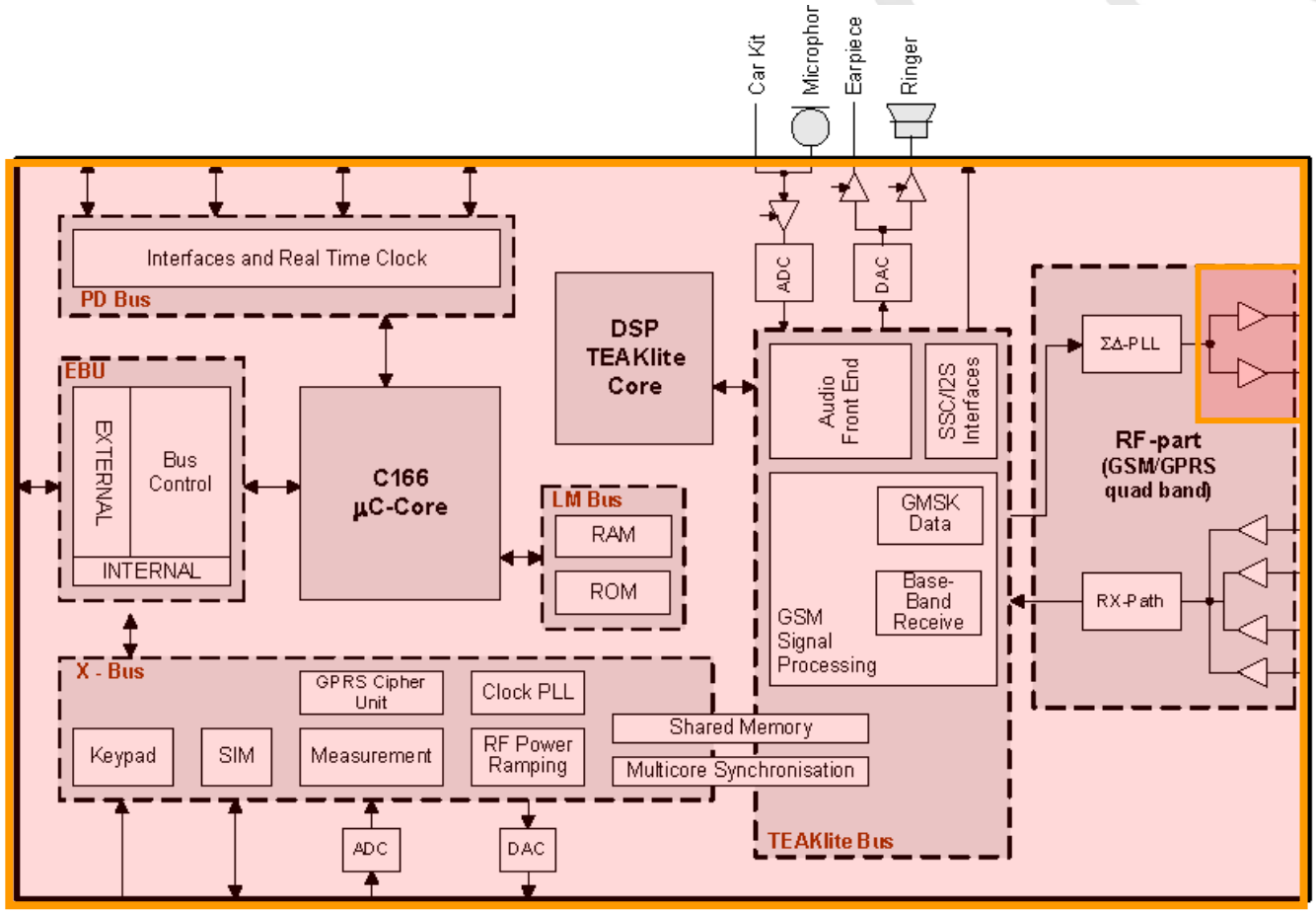
Technology Progression: GSM circa 1995



GSM Radio (transceiver) w/external components (e.g. filters)

Stetzler et al, ISSCC 95 (AT&T)

GSM: Today



GSM SoC with integrated transceiver and CPU

Bonnaud et al, ISSCC 06 (Infineon)

Beyond WiFi and Cellular

- Converged Devices of Today
  - Cellular handsets: GSM (CDMA) + camera + Bluetooth
  - Smart phones: PDA + GSM + Bluetooth + camera + WiFi
  - DSCs: camera + WiFi
  - PDAs: PDA + GPS + WiFi

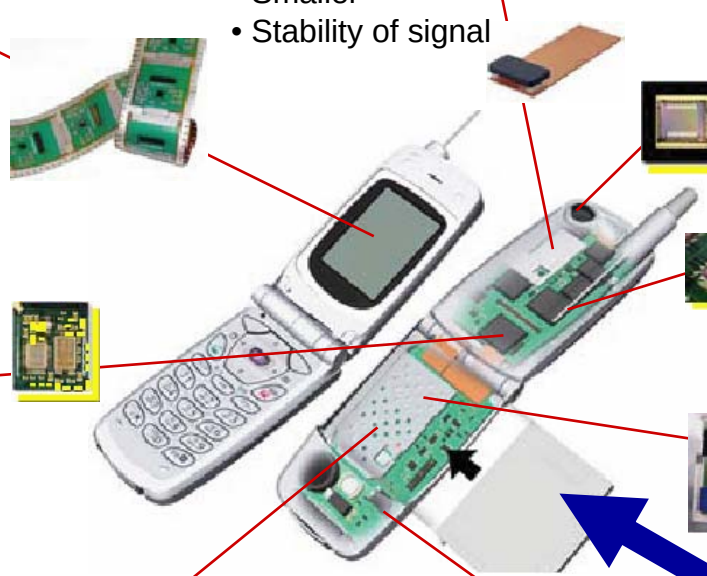
- Around the Corner
  - All of the above + DVB / Wireless USB / WiMax / WiMedia …

Market Trends

- Consumer Market Demands
  - More features (sooner) ⇨ complex designs, TTM
  - Thin/Sleek form factor ⇨ size
  - Longer battery life ⇨ low power

- What's the solution?
- System in a Package
- Maybe

What was in your Cell?



Embedded Antenna
- Smaller
- Stability of signal

LCD Circuit
- Larger display, Color display
- Lower power consumption
- Higher resolution

Camera Circuit
- Smaller
- Lower power consumption
- One unit of lens and control circuit

Memory Circuit
- Memory area for downloaded software
- Higher memory capacity

BB PHY/MAC/CPU
- Host CPU
- Application processor

Plug-In Memory Card
- Smaller, thinner
- Higher memory capacity

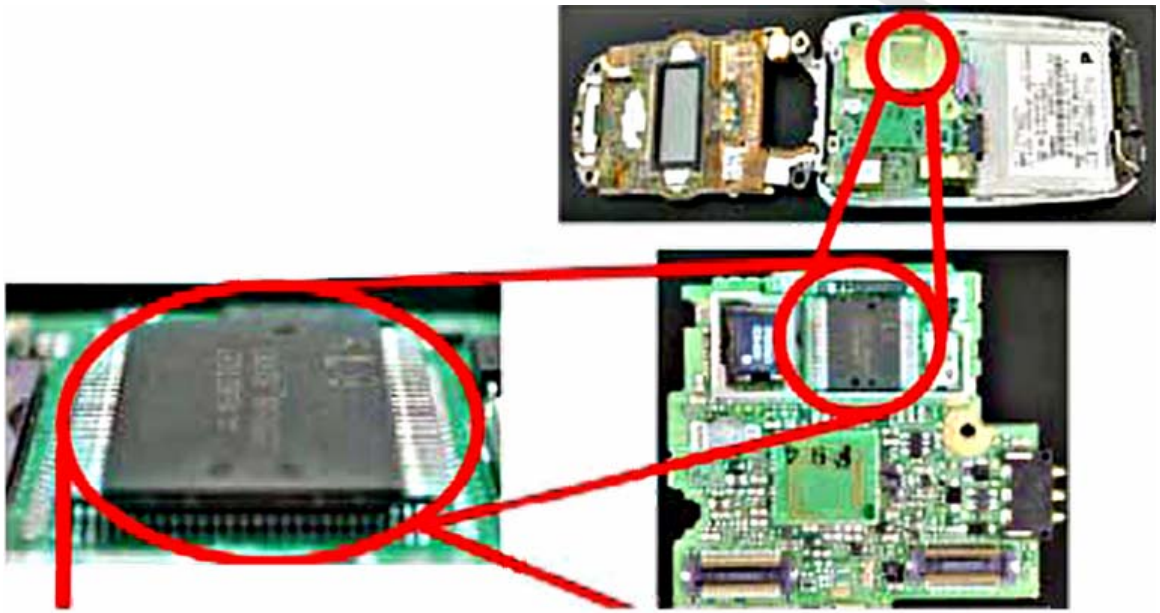
Outer Interface Circuit
- Bluetooth, USB Interface
- MP3, GPS Interface
- Memory Card Interface

Radio (FEM)
- Smaller and lower power consumption analog circuitry
- Decrease of # of mounted components

Power Supply Circuit
- Smaller size

Source: H. Ueda JEITA

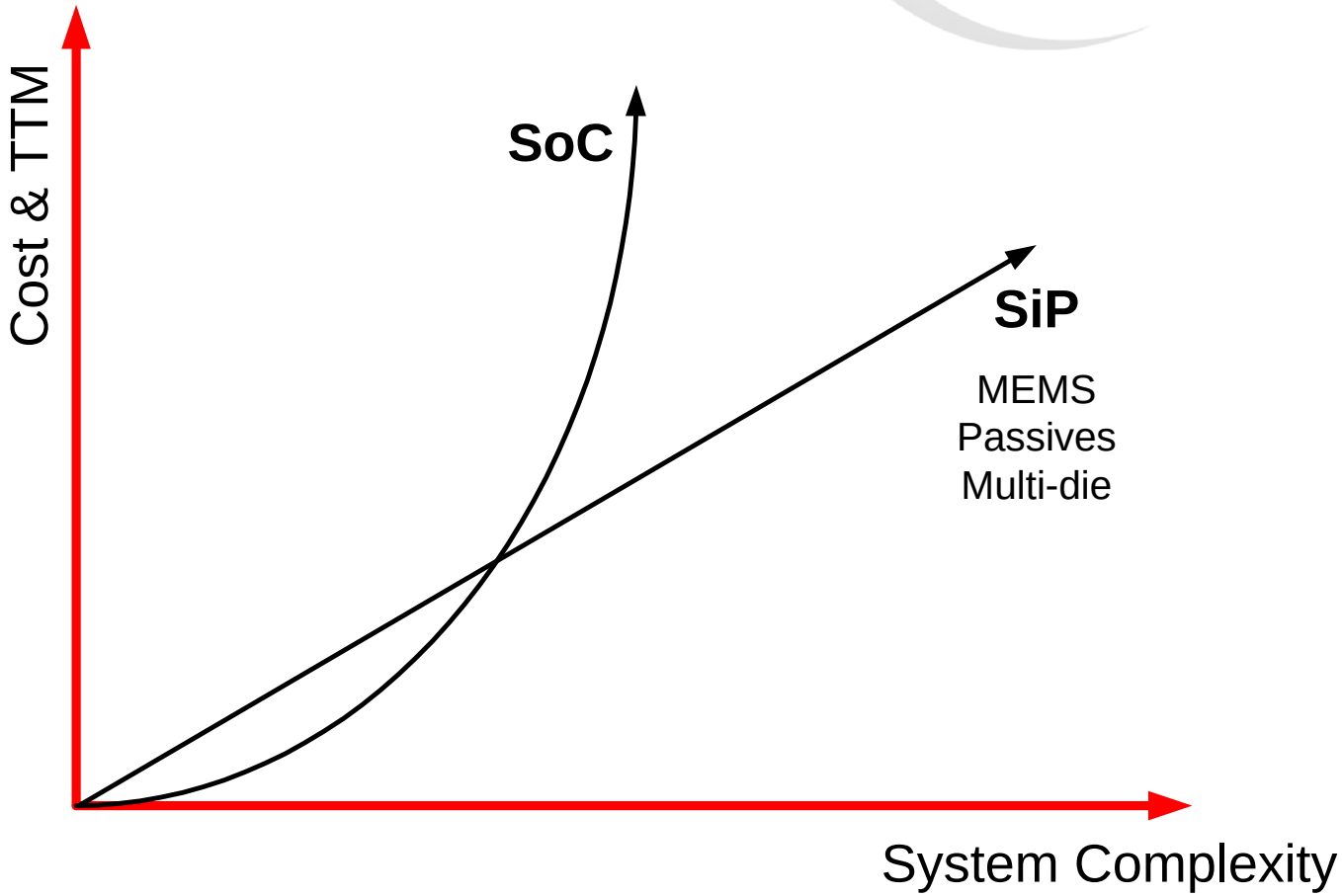
What's in your Smart Phone? SiP!



Cross-section of stacked 6-die package

Source: T. Sakura, Univ of Tokyo

System Integration



source: Fraunhofer IZM

Atheros, a WiFi Radio on a Chip Company

RoC Tradeoffs

- Advantages
  - Cost: die size and package
    - Single package
    - Fewer pads/pins
    - System reliability (fewer components)
  - Power
    - Fewer pads, fewer interconnect
  - Customer perception: single chip = cutting edge
  - Radio Performance
    - Digital calibration/tuning
      - I/Q imbalance
      - Tx Carrier leakage

RoC System Integration Tradeoffs

- Challenges
  - Radio design: Reduced external component count
    - Amplification: PA's and LNA's
    - Frequency translation: Mixers and VCOs
    - Frequency selection: still need high-Q filters
  - Radio performance
    - Digital noise coupling
      - Fully differential topology
      - Deep N-well isolation
      - Avoid pkg coupling to sensitive nodes (VCO) by keeping them on chip
    - Analog to analog noise coupling
      - Tools for layout analysis

Economic Decision Criteria

- Market size and product life time
- Wafer/package/die cost
  - Different technologies for radio vs. digital
  - Re-use possibilities
  - Multi-die packages add 25-35%
- Opportunity Cost
  - TTM
- Yield
  - 2 smaller die vs. 1 bigger die
  - Digital tuning/calibration

Technical Decision Criteria

- Technical Requirements & Engineering Feasibility
  - 2 die: Where to partition? Digital vs. Analog Interface?
    - Digital: parallel I/F (more pads, interconnect, power)
    - Digital: high speed serial (SERDES on each chip)
    - Analog (interconnect noise isolation, ADAC on digital chip)
  - Development effort (development cost)
  - System reliability (fewer components for RoC)

Decision Swayers

- Requirements for footprint
- Tools
  - Ultimate goal: Single TO
    - System-level DV
    - Radio performance simulation
- Flexibility of Design
  - Re-useable die vs. IP blocks
- Was RoC the correct decision?

What's Next for WiFi?

- Does RoC make sense for MIMO? 90, 65, 45nm… ?
  - Analog doesn't scale as easily as digital
  - Mix/Match for 2 die solution
  - Single chip vs. 2 die/1 pkg vs. 2 die/2 pkgs
    - If 2 die, where to partition
    - MIMO adds more interconnects – 2x, 3x, 4x
    - If single die, limitless interconnect possibilities
  - Economic drivers
    - Die cost
    - Opportunity cost
  - Engineering feasibility
    - Development cost

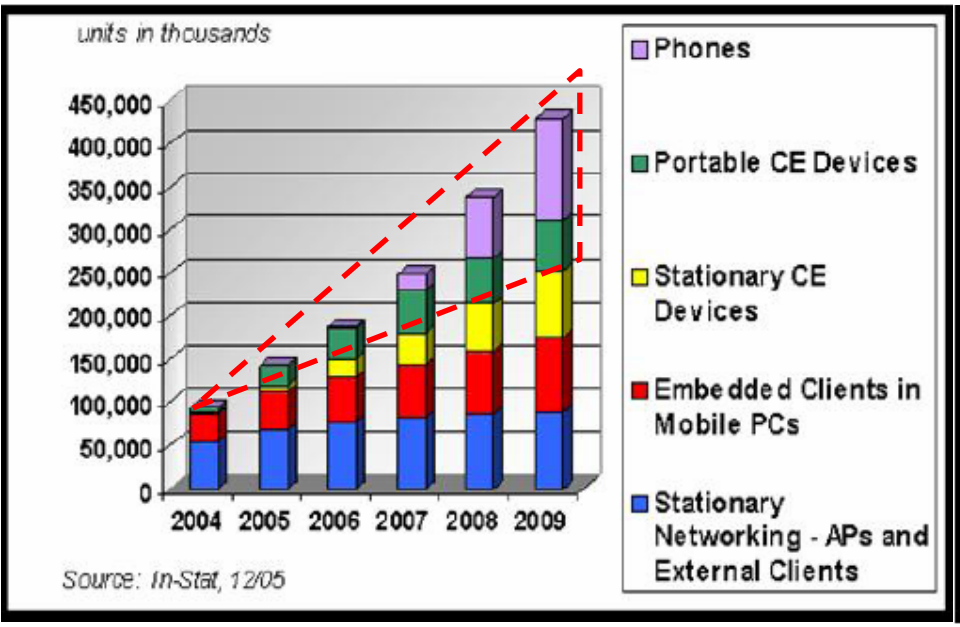
SiP Market Drivers for WiFi

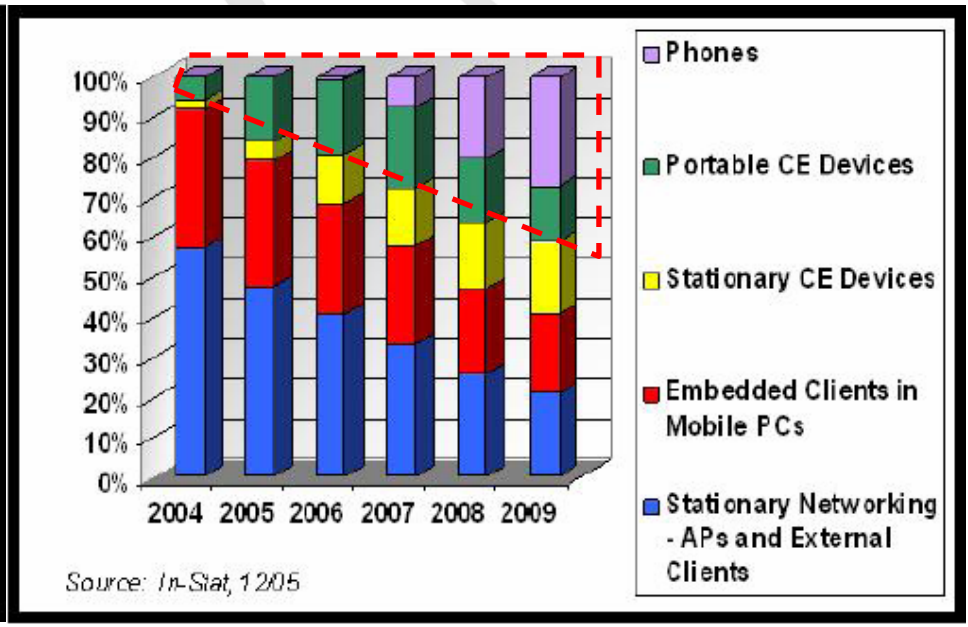
Convergence in Mobile CE Devices

Converged Devices = Platform + Features

Mobile CE	Platform	Features		
		Bluetooth	WiFi	Other
Cell phone	GSM/CDMA	✓	✓	GPS
PDA	Host CPU	✓	✓	GPS
DSC	Imaging		✓	
MP3 player	Media Player	✓	✓	
Gaming console	Host CPU	✓	✓	

Market Overview: Portable/Mobile CEs





Mobile CE Market Segments

Dual-mode Cellular/VOIP Phones

Mobile Gaming

Digital Cameras

Portable Media Players

WiFi for Portable/Mobile CEs

- New Market requirements
  - Low power
  - Small footprint
  - Package height
    - Thin is in
    - Stacked die may not be an option
  - Mechanical reliability (drop test)
  - “Plug and Play” system integration

“Single Chip” Mobile WiFi

- Component count
  - WLAN chip
  - Crystal
  - PA
  - LNA
  - FLASH
  - SAW
  - Other passives
- Simple solution: integrate with a SiP (Module)

SiP Tradeoffs

- **Advantages**
  - **“Plug & Play” system integration**
    - Layout
    - Test
    - Calibration
  - **TTM**
  - **Fewer Components**
    - Reliability
    - Yield
- **Challenges**
  - **Tools**
    - Signal Integrity
    - Mechanical Reliability (including thermal)
  - **Cost**
    - SiP package
    - Layout, test, calibration

Beyond WiFi

- Further Convergence
  - Bluetooth
  - WiMax
  - Wireless USB
  - WiMedia
  - GPS
- Integrate all “features” into a single platform
  - Mix/Match IP Die
  - “Plug & Play” integration
  - TTM

SoC for Converged Devices?

- SoC
  - Lower die cost
  - Lower power
- SiP
  - System houses want “best of all worlds”
    - Cost and performance
  - Features: “Moving target” standards
  - Development cost
  - Opportunity cost (TTM)
  - Manufacturability

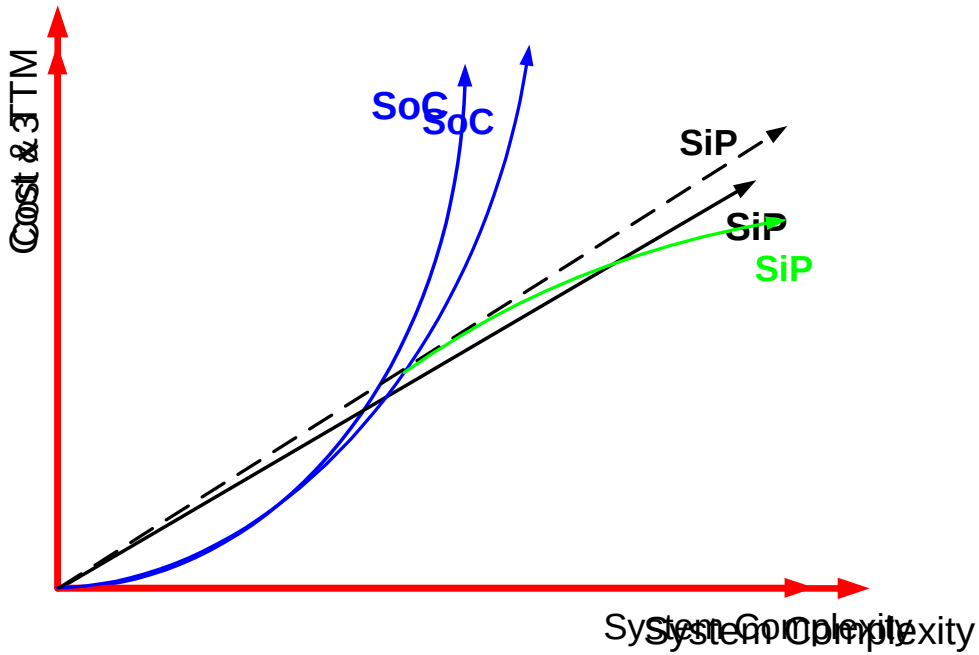
Pushing the SiP Envelope

- New Materials
  - “Green”
  - Flexible substrate
  - Low-κ / high-κ
  - Adhesives
- Tools Requirement
  - Database of New Materials
    - Mechanical
    - Electrical

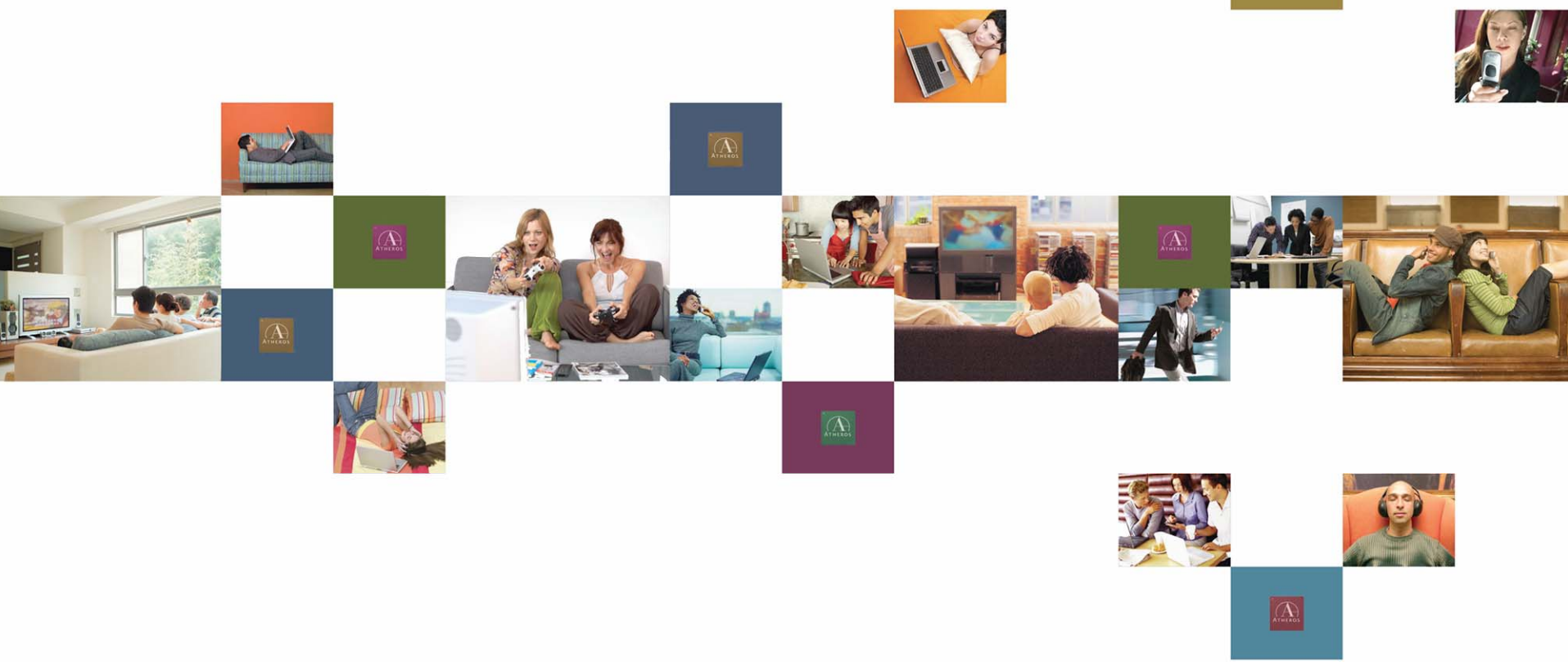
Summary: SiP vs. SoC

Decision Criteria

- Cost – die size (+ package)
- Cost – opportunity (TTM)
- Cost – development effort



Thank You



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